CLAIMS

What is claimed is:

1. A circuit for dynamically biasing an output stage of an op amp having a gain stage, comprising:

a first transistor (Q38), a second transistor (Q39), a third transistor (Q40), a fourth transistor (Q41), a fifth transistor (Q36), and a sixth transistor (Q37);

the first transistor (Q38) responsively coupled to and driven by current from the fifth transistor (Q36);

the second transistor (Q39) responsively coupled to and driven by current from the sixth transistor (Q37);

a seventh transistor (Q42) having a collector coupled to an emitter of the first transistor (Q38) and a base of the third transistor (Q40), and an emitter coupled to a first high impedance node operable to source current from the gain stage; and

an eighth transistor (Q43) having a collector coupled to an emitter of the second transistor (Q39) and a base of the fourth transistor (Q41), and an emitter coupled to a second high impedance node operable to sink current from the gain stage.

2. The circuit of Claim 1, further comprising the fifth transistor (Q36), sixth transistor (Q37), seventh transistor (Q42) and eighth transistor (Q43) sharing the same base-emitter connections;

the coupling of the fifth transistor (Q36), the sixth transistor (Q37), the seventh transistor (Q42) and the eighth transistor (Q43) being operable to force current from the fifth transistor

(Q36) and the seventh transistor (Q42) to substantially match, and current from the sixth transistor (Q37) and the eighth transistor (Q43) to substantially match.

3. The circuit of Claim 1, wherein the first transistor (Q38), the second transistor (Q39), the third transistor (Q40), the fourth transistor (Q41), the fifth transistor (Q36), the sixth transistor (Q37), the seventh transistor (Q42) and the eighth transistor (Q43) comprise bipolar transistors.

4. The circuit of Claim 3, wherein the first transistor (Q38), the fourth transistor (Q41), the fifth transistor (Q36) and the seventh transistor (Q42) comprise pnp type transistors; and

the second transistor (Q39), the third transistor (Q40), the sixth transistor (Q37), and the eighth transistor (Q43) comprise npn transistors.

5. The circuit of Claim 1, wherein the output stage forms a portion of class AB operational amplifier.

6. The circuit of Claim 5, wherein the circuit forms a portion of the op amp voltage feedback.

7. The circuit of Claim 5, adapted for use in an arbitrary waveform generator.

8. The circuit of Claim 5, adapted for use in a high linearity analog to digital converter ("ADC").

9. The circuit for dynamically biasing the output stage of an op amp of Claim 5, adapted as a digital to analog converter ("DAC") circuit.

10. The circuit of Claim 5, adapted for use in an output buffer circuit.

11. The circuit of Claim 5, adapted for use in an active filter circuit.

12. The circuit of Claim 5, adapted for use in a wireless communication receiver circuit.

13. An op amp circuit stage, comprising:

an input stage having at least one input and at least one output;

a common base gain stage having at least one input, and at least one output coupled to the output of the input stage;

an output stage including a pre-driver circuit coupled to the output of the common base gain stage; and

a dynamic biasing circuit operable to provide dynamic bias from the common base gain stage to the pre-driver circuit of the output stage.

14. The op amp circuit of Claim 13, wherein the dynamic biasing circuit further comprises:

a first transistor (Q38), a second transistor (Q39), a third transistor (Q40), a fourth transistor (Q41), a fifth transistor (Q36), and a sixth transistor (Q37);

the first transistor (Q38) being responsively coupled to and driven by current from the fifth transistor (Q36);

the second transistor (Q39) being responsively coupled and driven by current from the sixth transistor (Q37);

a seventh transistor (Q42) having a collector being coupled to an emitter of the first transistor (Q38) and a base of the third transistor (Q40), having an emitter being coupled to a first high impedance node operable to source current from the gain stage; and

an eighth transistor (Q43) having a collector being coupled to an emitter of the second transistor (Q39) and a base of the fourth transistor (Q41), and an emitter being coupled to a second high impedance node operable to sink current from the common base gain stage.

15. The op amp circuit of Claim 14, wherein the dynamic biasing circuit is operable to copy current from at least one node at the common base gain stage into the output stage to achieve high linearity.

16. An output stage of an op amp, comprising:

at least one pair of npn and pnp transistors arranged as pre-drivers;

at least one current source operable to source current from a gain stage of the op amp to the pnp transistor pre-drivers;

at least one current sink operable to sink current from the gain stage to the npn transistor pre-drivers; and

the current source and current sink responsively coupled to the pre-drivers so as to dynamically bias the pre-drivers.

17. A circuit for biasing pre-drivers of an op-amp output stage, comprising:

a first transistor (Q38), a second transistor (Q39), a third transistor (Q40) and a fourth transistor (Q41), a first current source and a second current source;

an emitter of the first transistor (Q38) being coupled to a base of the third transistor (Q40);

an emitter of the second transistor (Q39) being coupled to a base of the fourth transistor (Q41);

a base of the first transistor (Q38) being responsively coupled to and dynamically driven by current from the first current source; and

a base of the second transistor (Q39) being responsively coupled and dynamically driven by current from the second current source.

18. The circuit of Claim 17, further comprising:

the first current source comprising a fifth transistor (Q36);

the second current source comprising a sixth transistor (Q37);

a seventh transistor (Q42) having a collector coupled to an emitter of the first transistor (Q38) and a base of the third transistor (Q40), and an emitter being coupled to a first high impedance node operable to source current from a gain stage of the op amp;

an eighth transistor (Q43) having a collector coupled to an emitter of the second transistor (Q39) and a base of the fourth transistor (Q41), and an emitter being coupled to a second high impedance node operable to sink current from the gain stage;

the fifth transistor (Q36), sixth transistor (Q37), seventh transistor (Q42) and eighth transistor (Q43) sharing the same base-emitter connections; and

the fifth transistor (Q36), sixth transistor (Q37), seventh transistor (Q42) and eighth transistor (Q43) being operably coupled to force current from the fifth transistor (Q36) and the seventh transistor (Q42) to substantially match current from the sixth transistor (Q37) and the eighth transistor (Q43) to substantially match, respectively.

19. The circuit of Claim 17, further comprising a node capacitively coupling the bases of the first transistor (Q38) and second transistor (Q39) to a voltage rail.

20. The circuit of Claim 17, wherein the circuit is adapted for use in a class AB op amp circuit.

21. The circuit of Claim 17, wherein the transistors comprise bipolar transistors.

22. The circuit of Claim 21, wherein the first transistor (Q38), fourth transistor (Q41), fifth transistor (Q36) and seventh transistor (Q42) further comprise pnp-type transistors; and

the second transistor (Q39), third transistor (Q40), sixth transistor (Q37), and eighth transistor (Q43) further comprise npn-type transistors.